Ti/Au / n-GaAs planar Schottky diode with a moderately Si-doped matching sublayer

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November 2017

Abstract. In this paper we report on the results of the study of the Ti/Au / n-GaAs planar Schottky diodes (PSD) intended for the wideband detection of terahertz radiation. The two types of the PSD devices were compared having either the dual n/n_+ silicon dopant profile or the triple one with a moderately doped matching sublayer inserted. All the diodes demonstrated no noticeable temperature dependence of ideality factors and barrier heights, whose values covered the ranges of 1.2–1.5 and 0.75–0.85 eV, respectively. We observed the lowering of the flat band barrier height of ∼80 meV after introducing the matching sublayer into the GaAs sandwich. For both the devices types, the series resistance value as low as 20 Ohm was obtained. The measurements of the input frequency bandwidth within the range of 400–480 GHz were performed. The diodes demonstrated quite consistent frequency response regardless the type of the silicon dopant profile chosen, the cutoff frequency value of ∼655 GHz was evaluated. We also calculated the AC current density distribution within the layered structures similar to those being experimentally studied. It was demonstrated that insertion of the moderately Si-doped matching sublayer might be beneficial for implementation of a PSD intended for the operation within the 'super-THz' range.

Keywords: planar Schottky diode, matching sublayer, terahertz frequencies, input bandwidth, eddy currents

1. Introduction

The steady progress of terahertz applications [1] stimulates the implementation of new and development of existing technologies for both radiation sources and receivers. At the moment, several basic technologies can be employed for the heterodyne detection of a terahertz radiation. Thus, the superconductor-insulator-superconductor (SIS) mixer is extremely efficient at frequencies below 1.4 THz [2], the superconducting hot electron bolometric (HEB) mixer can be used above that frequency and has no competitors in the sensitivity within the 'super-THz' range (i.e. 3–6 THz) [3], and the input frequency bandwidth of the planar Schottky diode (PSD) mixer is limited by ∼3 THz from the upper side [4]. In contrast to the superconducting technologies of the SIS and HEB mixers, the latter technology is based on semiconductors and is mainly associated with the use of layered GaAs-based structures, which do not imply usage of bulky and expensive cryogenic equipment to achieve decent noise performance. The lack of need to cool the PSD down to helium temperatures makes it quite attractive for practical applications. Moreover, the technology of planar diodes, unlike whisker contacted diode technology, allows to strictly control parameters of the devices being fabricated and enables easy way of integrating them with complex high-frequency circuits. But despite numerous advantages, the planar technology has certain drawbacks associated with appearance of a series resistance and shunt capacitance in the diode's intrinsic circuitry. In case of the surface channel PSD, eddy currents induced in its layered structure also greatly affect the performance at terahertz frequencies [5]. The effect of eddy currents is ruled by the topology and takes place in the devices utilizing relatively thick mesas. In terms of equivalent circuit of PSD, this can be represented as a series-connected inductance, which implies certain limits on the diode's input bandwidth. The effect, however, can be suppressed by reducing the mesa thickness downto somewhat comparable with the skin depth at given frequency. But at the submicron thicknesses this manipulation might lead to significant increase of the complexity of structuring the diode.

In this paper, we propose to use a sequence of epitaxial GaAs layers with smoothly varying doping levels within the sandwich to build up a PSD for the terahertz operation. This is to potentially mitigate the effect of eddy currents along with the skin and proximity effects having a diode with ∼60 % thicker mesas compared to the conventionally used PSD devices.

Table 1. The layer structure of the MBE grown GaAs wafers. Here t is the thickness and N is the doping level.

Type	Layer #	Designation/composition	t, μm	N, cm^{-3}
1	4	n-GaAs	0.2	4×10^{17}
	3	n_+-GaAs	1.2	5×10^{18}
	2	$Al_xGa_{1-x}As^*$	0.05	–
	1	GaAs sublayer	0.03	–
	0	i-GaAs(100) substrate	350	–
2	5	n-GaAs	0.15	4×10^{17}
	4	n′-GaAs	0.06	1×10^{18}
	3	n_+-GaAs	0.8	5×10^{18}
	2	$Al_xGa_{1-x}As^*$	0.05	–
	1	GaAs sublayer	0.03	–
	0	i-GaAs(100) substrate	350	–

$^*x = 0.8 \pm 0.04$.

2. Fabrication of the PSD samples

In our studies we used two types of the Si-doped GaAs based heterostructures grown by the means of molecular beam epitaxy (MBE). Detailed information on the heterostructures' properties is summarized in table 1.

The both types of wafers comprise a handle consisting of a thick isolating GaAs substrate followed by a thin GaAs sublayer with $Al_{0.8}Ga_{0.2}As$ etch stopper atop of it. For the structures of type 1, the handle is followed by a 1.2 μm thick n_+-GaAs layer with a doping level of 5×10^{18} cm^{-3}. The next sublayer of the structure is presented by a 0.2 μm thick n-GaAs layer with a doping level of 4×10^{17} cm^{-3}. The structures of type 2 also contain the n_+- and n-GaAs layers possessing identical doping levels and similar thicknesses (0.8 μm and 0.15 μm respectively) compared to that of the type 1. However in contrast to the latter, an n′-GaAs sublayer is introduced as an transition from n_+- to n-GaAs. This transitional layer is a Si-doped up to a level of 1×10^{18} cm^{-3} and has a thickness of 0.06 μm.

The both types of the MBE grown GaAs wafers were processed within the same fabrication routine, which mostly makes use of photo- and e-beam lithographies, resistive thermal evaporation and selective GaAs/AlGaAs wet etching to define the diode's cathode and anode mesas along with a spiral antenna attached to them. In our work we chose to implement a surface channel PSD [4]. Referring to figure 1, the fabrication process includes six essential steps:

(i) Deposition of a 50 nm thick SiO_2 mask on top of the n-GaAs layer.

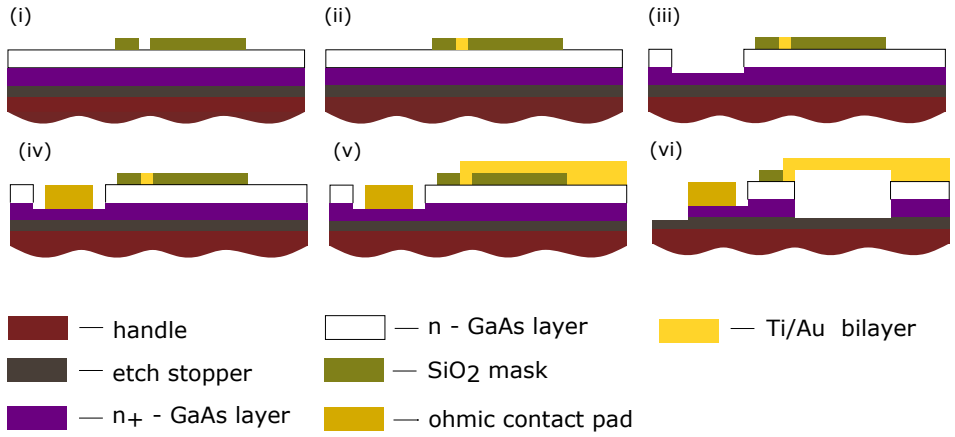

Figure 1. Main stages of the PSD fabrication process.

(ii) Formation of the Schottky contact. The space charge region of the PSD is formed as an interface between the n-GaAs layer and thin Ti/Au (10/65 nm) bilayer deposited on top of it. A circular opening of certain diameter presenting in the SiO_2 mask fabricated by dry etching through the resist pattern defines the PSD anode area. In our studies anode's diameter (D_A) stayed within the range of 1–3 μm. As one can notice, thickness of the mask determines height of the Ti/Au rod.

(iii) Local removal of the n-GaAs layer (and also the n′-GaAs layer in case the wafers of type 2) in vicinity of the ohmic contact being further implemented.

(iv) Formation of the cathode lead, which is presented by a section of the n-GaAs layer that starts at the position of the Schottky contact and ends up by the ohmic contact pad. The latter is implemented as the Ni/Ge/Au/Ni/Au (5/20/35/15/80 nm) multilayer metallization system in a manner similar to that described in [6]. The cathod lead is meant to provide a transition between the space charge region and the feed of spiral antenna being further implemented, consequently, to provide a path for transport current to flow through the PSD structure.

(v) Fabrication of inner and outer pads of the spiral antenna made of the Ti/Au bilayer. The inner pads are presented by the antenna's feed of a micro scale integrated with the anode lead, which links the Schottky contact and opposite arm of the antenna. In out work, its length and width are fixed to 22 and 1.1 μm,

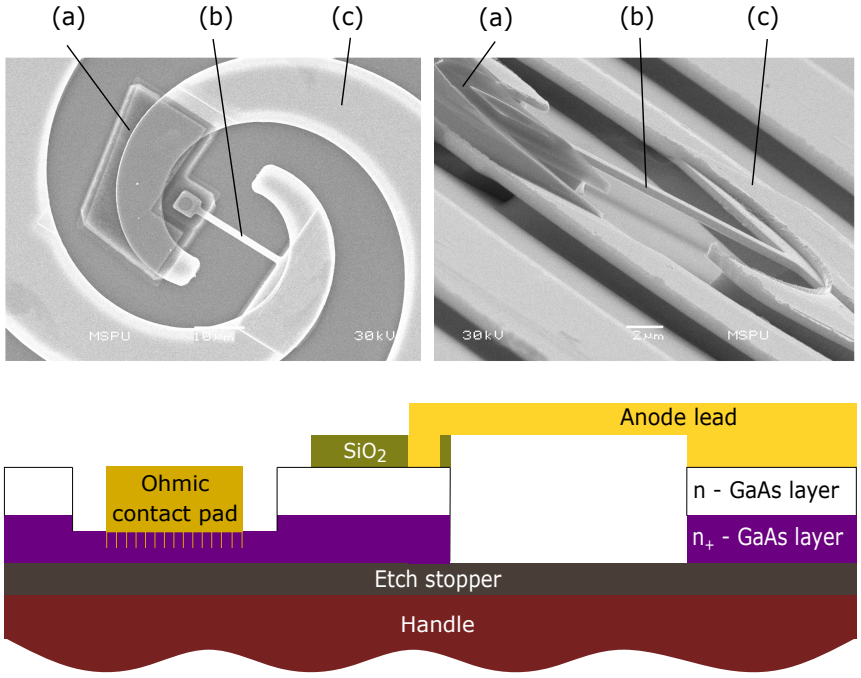

Figure 2. SEM images containing top (top panel, left) and side (top panel, right) views of a quasioptical PSD, and a schematic of its layered structure (bottom panel). Here (a), (b) and (c) denote the ohmic contact pad, the anode lead and the antenna arm, respectively.

respectively.

(vi) Formation of the groove separating the PSD's anode and cathode mesas via etching of the SiO_2 mask along with the unprotected n- and n_+-GaAs layers (under the cathode lead being simultaneously transformed into a suspension bridge).

Scanning electron micrographs (SEM) of a typical PSD sample produced are provided in figure 2. The figure also contains a schematic cross-sectional view (not to scale) of the sample's layered structure.

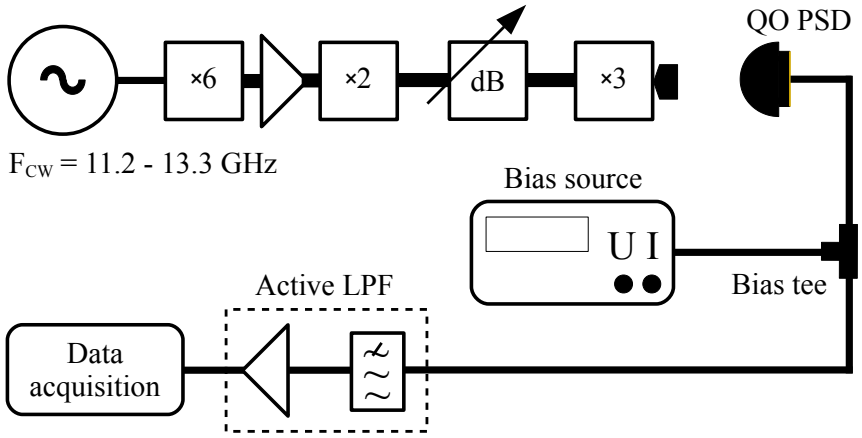

Figure 3. Experimental setup.

3. Experimantal setup and methods employed

Referring to figure 3, chip of the PSD sample was glued to a hemispherical Si lens, which was installed into a holder equipped with an sma connector attached to the outer pads of the PSD's antenna through the coax-to-coplanar transition. The sample holder was further connected to a bias tee, DC port of which was attached to a source meter employed to bias the PSD and to measure transport current through its layered structure simultaneously.

3.1. DC characterization

In order to evaluate basic DC parameters of the samples produced, we employed a standard analysis of the current-voltage (IV) characteristics. It is known that forward branch of the IV characteristic of the Schottky diode starting from the $V_d > 3\,k\,T/q$ and up to the end of the low voltage range, i.e. where drop of the bias voltage on the series resistance (R_s) is negligible compared to that of on the space charge region (figure 4), in the semi-log scale should obey a linear dependence law, and it can be expressed by an 'ideal IV curve'

$$ln(I_{id}(V_d)) = a\,V_d + b. \tag{1}$$

Hereinabove V_d is the DC voltage applied to the diode, q is the electron charge, k is the Boltzmann constant and T is the diode's physical temperature.

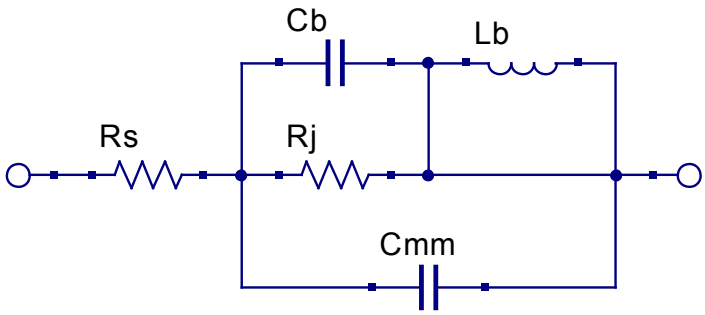

Figure 4. The lumped element model of the inner part of the PSD sample. Here R_s is the series resistance, R_j is the junction resistance, L_b is the inductance of the suspension bridge, C_b and C_{mm} are the 'bridge-to-mesas' and 'mesa-to-mesa' capacitances, respectively

At the same time based on the thermionic-field emission model [7] the transport current within the low bias voltage range can be calculated as

$$I_{id}(V_d) \approx I_s \, exp\left(\frac{q\,V_d}{\eta\,k\,T}\right). \tag{2}$$

Thus, based on the measurement of the diode's IV curve its ideality factor and saturation current can be calculated as $\eta = q\,(a\,k\,T)^{-1}$ and $I_s = exp(b)$, respectively. The latter value is further used to calculate the zero bias current barrier height (Φ_{b0})

$$\Phi_{b0} = k\,T/q \cdot ln(A^{**}A\,T^2/I_s), \tag{3}$$

where A^{**} is the effective Richardson constant, A is the area of the Schottky contact. To account for natural lowering of the barrier height, an addend presented by the image force correction ($\Delta\Phi_{bi}$) to equation 3 can be introduced. $\Delta\Phi_{bi}$ is calculated to be ∼40 meV for the n-type contacts employed [8, 9].

Making use of the η and Φ_{b0} values previously obtained, one can calculate the flat band barrier height (Φ_{bf}) of the Schottky contact as

$$\Phi_{bf} = \eta\,\Phi_{b0} - k\,T(\eta - 1)/q \cdot ln(N_c/N_d), \tag{4}$$

where N_d is the doping concentration in the semiconductor and N_c is the effective density of states in the conduction band. During the calculations we account for the temperature dependence of the latter parameter.

Beyond the low voltage range, where drop of the bias voltage on R_s can no longer be neglected, deviation of the experimental IV curve from the ideal shape can be used to calculate the series resistance value. Redistribution of voltages between the space charge region and series resistance within the PSD's layered structure can be expressed via 'real IV curve'

$$I_{re}(V_f) = I_s \left[exp\left(\frac{q\, V_j(V_f)}{\eta\, k\, T} \right) - 1 \right], \tag{5}$$

where $V_j(V_f) = V_f\,(1 - R_s/R_f(V_f))$. Here V_f is the voltage applied to the whole diode structure, V_j is the voltage incident to the space charge region and R_f is the total resistance of the diode (index 'f' denotes forward branch of the IV curve). Using R_s as a parameter to best fit the IV_{re} function to the experimental outcome by the method of least squares, one can evaluate its actual value.

3.2. Response at high frequencies

We combined a frequency synthesizer with chain of frequency multipliers to implement a terahertz source of the amplitude-modulated (AM) CW signal, which was fed into the PSD to probe its response. The modulation frequency was set to 1.5 kHz during all the measurements. Response signal of the PSD to the incident terahertz power was transferred through a high frequency (HF) branch of a wideband bias tee and further amplified by an active low-pass filter (LPF) with a gain of 74 dB and frequency bandwidth of 30 kHz. Then, the amplified signal was recorded by a data acquisition operated at the sampling rate of 100 kHz. To distinguish the AM response component in the output spectrum of the PSD, we applied a Fourier transform algorithm to the digitized signal.

4. Results and discussion

To study transport properties of the diodes, we performed analysis of their IV curves obtained in the temperature range of 295–395 K. Figure 5 contains family of the IV curves with the temperature behavior typical for the samples produced. The best values of ideality factors achieved for the both types of the PSD samples within the fabrication process developed were in the range of 1.15–1.25, the corresponding series resistances were around 20 Ohm. The antenna coupled diodes had slightly worse characteristics in terms of η and R_s compared to that of the antenna free diodes. The room temperature values of the barrier height Φ_{bf} covered the range of ∼0.75–0.85 eV.

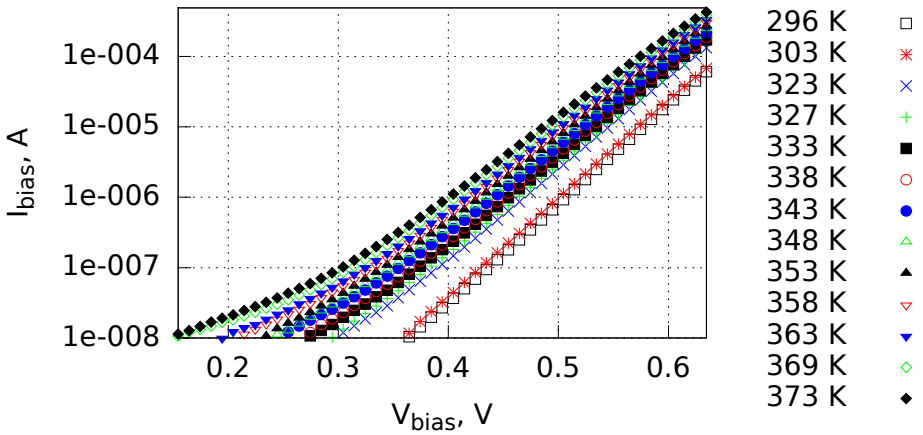

Figure 5. IV curve as a function of the diode's operating temperature. Y-axis is given in the logarithmic scale.

4.1. Properties of the Schottky barrier

Assuming the Gaussian distribution of the Schottky barrier height, one can define the Φ_{b0} value as [10]

$$\Phi_{b0} = \Phi_m - \sigma_s^2 \, q \, (2kT)^{-1}, \tag{6}$$

where Φ_m is the mean barrier height, which can be measured by the capacitance-voltage (CV) method, σ_s is the standard deviation of the barrier height distribution. The latter parameter is temperature dependent, namely, $\sigma_s^2(T) = \sigma_s^2(0) + \alpha_\sigma T$ [11]. In addition, it is generally stated that the flat band barrier height is basically the same as the barrier height obtained through the CV method [12, 13]. As a result, equation 6 takes the form

$$\Phi_{bf} - \Phi_{b0} = \sigma_s^2(0) \, q \, (2kT)^{-1} + \alpha_\sigma \, q \, (2k)^{-1}. \tag{7}$$

Thus, homogeneity of the Schottky barrier can be verified through comparing the Φ_{bf} and Φ_{b0} values, whose difference inversely depends on temperature. As one can notice, the slope and intercept of this linear function can be employed to define values of the standard deviation at zero temperature ($\sigma_s(0)$) and the temperature coefficient (α_σ).

Figure 6 provides the experimental dependencies $\Delta\Phi(T^{-1}) = \Phi_{bf} - \Phi_{b0}$ for the samples of type 1 and type 2 which equal to $0.0034\,T^{-1} + 0.127$ and $0.0061\,T^{-1} + 0.265$,

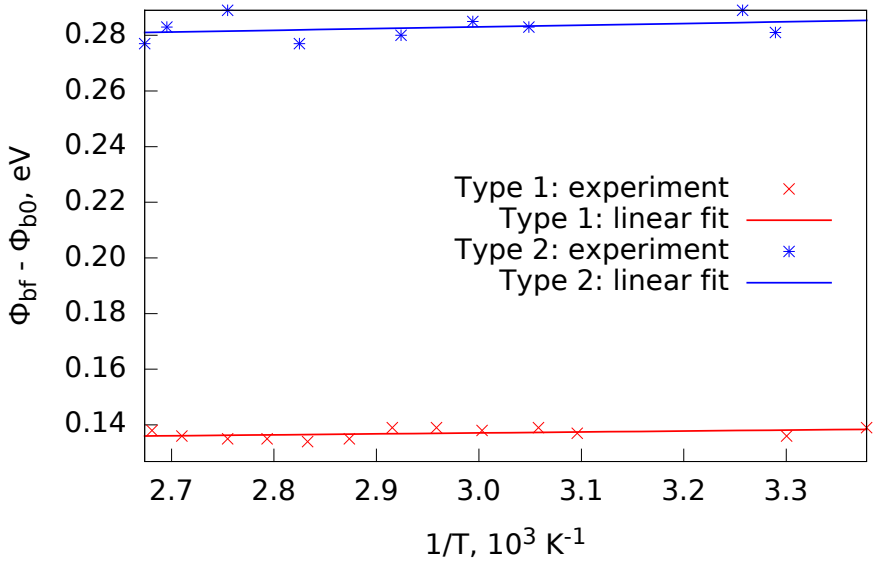

Figure 6. The difference of the flat band and the zero bias current barrier heights as a function of the inverted operating temperature of the PSD sample.

Table 2. Parameters of the quasioptical PDSs employed for the AC measurements.

Sample	D_A, μm	η	R_s, Ohm*	Φ_m, eV,	σ_s, meV
1 (type 1)	3	1.2	20	0.840	80
2 (type 2)	3	1.5	50	0.762	116

*The DC resistance of antenna is subtracted.

respectively. The experiment yielded that the difference of the barrier heights barely depends on temperature. The same temperature behavior was also observed for the barrier heights themselves and for the samples' ideality factors.

4.2. Frequency response

The basic parameters evaluated through the analysis of the room temperature IV characteristics (figure 7) of the samples employed for the AC measurements are summarized in table 2. These measurements were conducted to validate the calculated values of the PSDs' parasitic parameters and to experimentally determine the cutoff frequencies of their operational ranges.

During the measurements, the bias voltage corresponding to the transport current value of ∼500 μA was applied to each PSD to increase its responsivity. The linearity

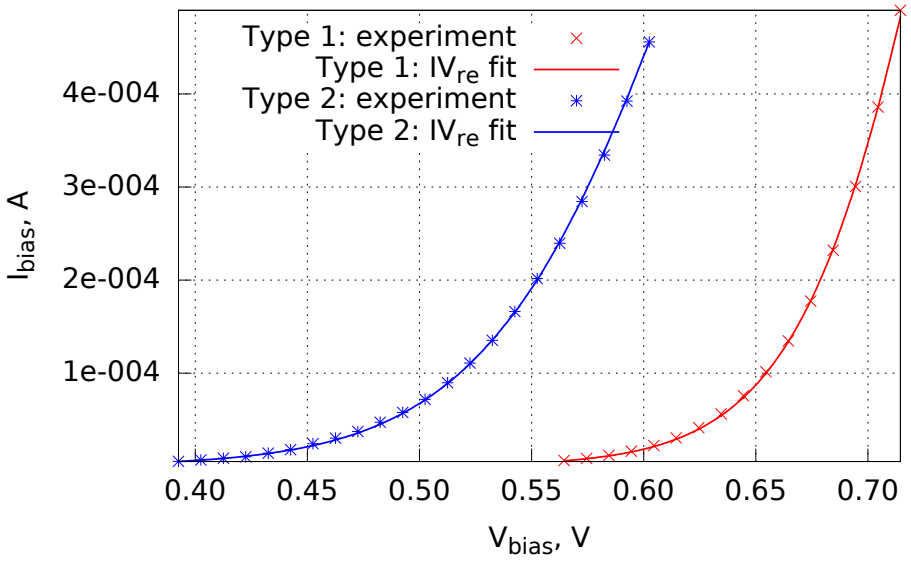

Figure 7. The IV curve of the PSD sample measured at ambient temperature.

range of the samples within the experimental setup used was equal to 25 dB on average and was mainly limited by the noise floor of the electronic readout system. The measurements were carried out with the PSDs being operated around the middle of the linearity range. Therefore, the ripples of the terahertz source's power of ∼6 dB caused by the frequency sweep did not result in distortion of the measurement results due to the saturation effects.

The samples were implemented in a quasioptical manner. We employed the on-chip circuitry mostly associated with the use of the equiangular spiral antenna to couple terahertz signal to the surface channel structure of the diode. Based on the antenna geometry, the lower and upper frequency limits of its operational range can be calculated via equations 8 and 9, respectively [14].

$$f_{min} = c/n_{eff} \cdot (\rho_{max} - \rho_0)^{-1}(4\pi^2/ln^2(\epsilon) + 1)^{-0.5} \quad (8)$$

$$f_{max} = c/n_{eff} \cdot (4\rho_0)^{-1} \quad (9)$$

Here c is the speed of light, n_{eff} is the effective refractive index at the substrate/vacuum interface, ρ_0 and ρ_{max} are the inner and outer radii of the spiral correspondingly equal to 29 and 178 μm for the antennas used. The expansion ratio (ϵ) of the spiral is equal to 2.73. Thus, one can conclude that the input frequency bandwidth of such an antenna implemented on the GaAs substrate covers the range of 120–980 GHz. At the middle of this range, the match of the antenna and the surface

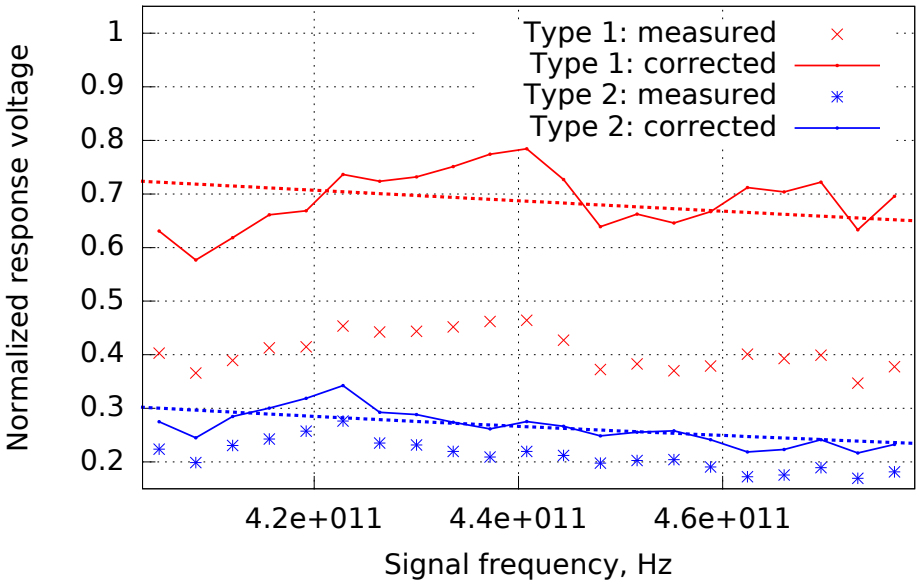

Figure 8. Response voltages of the quasioptical PSD samples as a function of the signal source's frequency. The dotted lines denote the corresponding RC fits.

channel structure of the diode can be presented in terms of the reflection coefficient as

$$\Gamma(f) = (Z_{RLC} - Z_a)(Z_{RLC} + Z_a)^{-1}, \tag{10}$$

where Z_a is the antenna impedance, $Z_{RLC} = R_s + (R_j^{-1} - iX_{Ctot}^{-1})^{-1}$ and $C_{tot} = C_b + C_{mm}$. In contrast to the DC characterization case, here R_j is treated as the junction differential resistance. The inductance of the suspension bridge is considered as the inductance of a flat wire [15, 16]. Based on the geometry chosen, it equals to 17.2 pH for the both samples and its contribution to Z_{RLC} can be neglected at the discussed frequencies. Finally, the power incident to the PSD's intrinsic RC circuitry can be written as

$$P_{inc}(f) = 1 - |\Gamma|^2. \tag{11}$$

We calculated the antenna impedance in High Frequency Structure Simulator (HFSS) within the setup already used by us in the past [14]. The antenna resistance was close to 50 Ohm and barely depended on frequency, while the reactance demonstrated almost purely inductive behavior corresponding to the inductance value of 6.4 pH. Thus, at 450 GHz $Z_a = 49.6 + i\,18$ Ohm.

To extract the total parasitic capacitance (C_{tot}), we performed the Y-parameters analysis within the electromagnetic (EM) modeling of the samples' behavior with the

help of HFSS. The evaluation procedure was similar to that described in [5]. The 3d model of a PSD we used for the calculation was based on the geometry of its layered structure discussed in details in section 2. The calculated values of C_{tot} were equal to 12.2 and 12 fF for the samples 1 and 2, respectively. The samples also possessed the differential resistances of 105 and 210 Ohm in vicinity of the bias voltages chosen. Thus, at 450 GHz $Z_{RLC1} = 27.5 - i\,26.9$ and $Z_{RLC2} = 54 - i\,28.9$.

Figure 8 contains experimental dependencies of the PSD samples' response voltages on the frequency of the input signal within the range of 400–480 GHz. The experimental data was normalized by the $P_{inc}(f)$ function and was further fitted by the gain of the RC circuit associated with decoupling of the space charge region with the signal power due to the leakage of the latter through the parasitic capacitance. We observed a decent agreement of the RC fits with the normalized response voltages of the samples which validates the extracted values of the parasitic parameters. Consequently, the upper frequency limit (F_c) of the PSD's operational range in case of proper input optics can be calculated as

$$F_c = (2\pi\, R_s\, C_{tot})^{-1}. \tag{12}$$

Substituting the corresponding parasitic parameters into equation 12, we get the cutoff frequencies $F_{c1} = 650$ GHz and $F_{c2} = 265$ GHz for the samples 1 and 2, respectively. It is necessary to note that the excess value of the series resistance of the sample 2 is due to moderate overetching of the n_+-GaAs layer during the fabrication procedure. Moreover, the antenna free devices of type 2 demonstrated the R_s value as low as 20 Ohm. Therefore, it can be concluded that in general case F_{c2} can be shifted up to 660 GHz meaning that the samples demonstrate quite consistent frequency response regardless the type of the GaAs-based wafer chosen.

4.3. Mitigation of the high frequency losses

At frequencies beyond a few hundred gigahertz, one has to consider contribution of the eddy currents along with the skin and proximity effects to the total losses limiting the performance of a PSD. Generally speaking, these negative effects are geometry dependent and can be mitigated, once the thickness of the current-carrying GaAs layer is set to the skin depth at given frequency. In case of our PSD samples, this layer is presented by the heavily doped n_+-GaAs (sample 1) and the mixture of the moderately doped n'- and heavily doped n_+-GaAs (sample 2). The difference of the doping levels results in different conductivities. Thus, values of the bulk conductivity of the n'- and n_+-GaAs layers are equal to 29.2 and 146 S/mm which correspond to the skin depths (δ) of 4.4 and 2 μm at 450 GHz, respectively. As one can notice, the PSD samples we employed for the AC measurements possessed the current-carrying

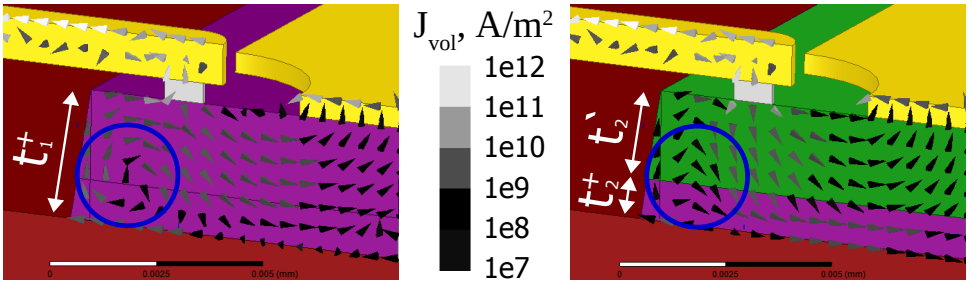

Figure 9. The calculated current density distribution within the layered structure of a PSD of type 1 (left) and type 2 (right) at 450 GHz. The coloring is identical to that provided in figure 1 except for the additional 'green' layer denoting the n′-GaAs matching sublayer.

layer thicknesses approximately equal to $\delta/2$. This fact allows to conclude that the eddy currents effect was mitigated, while the impact of the skin and proximity effects on the spread resistance was pronounced [5]. We did not account for that during the discussion of the AC measurements results, because distortion of the samples' frequency responses profiles due to those effects is negligible within the frequency range of interest.

Figure 9 provides the current density distribution within the PSDs' layered structures calculated in HFSS. For the calculation, we used the 3d models reflecting structural properties of the samples up to the thicknesses of the current-carrying layers. We chose these thicknesses to be equal for the structures being modeled. For the structure of type 2, thicknesses of the n′- and n_+-GaAs layers were set to a half skin depth each which gives $t_2' = 2.2$ μm, $t_2^+ = 1$ μm and $t_2' + t_2^+ = \delta$. In case of the structure of type 1, thickness of the n_+-GaAs layer was set to 3.2 μm meaning that $t_1^+ = 1.6\,\delta$. It can be clearly seen from the plot that the perturbations of AC current inside the current-carrying part of the structure 2 are mild compared to that of the structure 1. We propose that this feature can be employed to implement a PSD utilizing $\sim$ 60% thicker mesas without compromising its performance due to the mechanisms of the high frequency losses described hereinabove. Considering the complexity of structuring the diode with the submicron mesa thickness, the layout proposed should give more flexibility and be quite beneficial in case of a PSD intended for the operation within the 'super-THz' range.

5. Conclusion

We conducted a series of measurements and calculations focused on the exploration of the performance of the Ti/Au / n-GaAs PSD devices of various typologies. The diodes of two types were compared having either the dual n/n_+ silicon dopant profile or the triple one with a moderately doped matching sublayer inserted. While not demonstrating significant difference in terms of the quality of a Schottky barrier, the devices of both types possessed parasitic parameters suitable for the efficient use of the diodes at frequencies up to ∼655 GHz. Based on the EM modeling results, we also proposed that insertion of the moderately Si-doped matching sublayer into the GaAs sandwich is beneficial to mitigate the high frequency losses within the 'super-THz' range.

Acknowledgments

Boris Voronov acknowledges financial support from the Ministry of Education and Science of the Russian Federation through a State Task # 11.2423.2017/4.6.

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